CLAIMS

The invention claimed is:

1. A CMOS inverter comprising:

a first transistor device supported by a semiconductor substrate; and

a second transistor device over the first transistor device.

2. The inverter of claim 1 wherein the CMOS inverter comprises an SOI construction supported by a substrate.

3. The inverter of claim 2 wherein the substrate comprises a semiconductive material.

4. The inverter of claim 2 wherein the substrate comprises glass.

5. The inverter of claim 2 wherein the substrate comprises aluminum oxide.

6. The inverter of claim 2 wherein the substrate comprises silicon dioxide.

7. The inverter of claim 2 wherein the substrate comprises a metal.

8. The inverter of claim 2 wherein the substrate comprises a plastic.

9. The inverter of claim 1 wherein:

the first transistor device is a PFET device; and

the second transistor device is an NFET device.

10. The inverter of claim 1 wherein:

the first transistor device is an NFET device; and

the second transistor device is a PFET device.

11. The inverter of claim 1 wherein:

the first transistor device comprises a first gate;

the second transistor device comprises a second gate; and

the second gate is directly over the first gate.

12. The inverter of claim 1 wherein the first transistor device comprises source/drain regions extending into an SOI construction.

13. The inverter of claim 1 wherein the second transistor device comprises source/drain regions extending into an SOI construction.

14. The inverter of claim 1 wherein the first and second transistor devices comprise source/drain regions extending into SOI constructions.

15. The inverter of claim 1 wherein:

the first transistor device comprises a first gate and a pair of first source/drain regions proximate the first gate;

the second transistor device comprises a second gate and a pair of second source/drain regions proximate the second gate;

the second source/drain regions are directly over the first source/drain regions; and

the second gate is directly over the first gate.

16. A CMOS inverter comprising:

a first transistor device supported by a semiconductor substrate, the first transistor device comprising a first gate and a pair of first source/drain regions proximate the first gate, the first transistor device being a PFET device and the first source/drain regions accordingly being p-type doped regions;

a layer of semiconductive material over the first transistor device; and

a second transistor device supported by the layer of semiconductive material, the second transistor device comprising a second gate and a pair of second source/drain regions proximate the second gate, the second transistor device being an NFET device and the second source/drain regions accordingly being n-type doped regions; the second source/drain regions extending into the layer of semiconductive material.

17. The inverter of claim 16 wherein the second gate is directly over the first gate.

18. The inverter of claim 16 wherein the second source/drain regions are directly over the first source/drain regions.

19. The inverter of claim 16 wherein the semiconductor substrate comprises a material containing silicon and germanium, and wherein the first source/drain regions are p-type doped regions of the material containing silicon and germanium.

20. The inverter of claim 19 wherein the material containing silicon and germanium is n-type doped between the first source/drain regions.

21. The inverter of claim 16 further comprising a p-type doped vertically extending pillar in electrical contact with one of the first source/drain regions and also in electrical contact with the layer of semiconductive material.

22. The inverter of claim 16 further comprising a p-type doped vertically extending pillar in physical contact with one of the first source/drain regions and also in physical contact with the layer of semiconductive material.

23. The inverter of claim 22 wherein the layer of semiconductive material has a bottom surface extending substantially horizontally, and wherein the vertically extending pillar extends substantially perpendicular to said bottom surface.

24. The inverter of claim 22 wherein the second source/drain regions are directly over the first source/drain regions.

25. The inverter of claim 24 wherein the p-type doped vertically extending pillar physically contacts the layer of semiconductive material at a location directly under one of the second source/drain regions; and wherein the layer of semiconductive material is p-type doped at the location where the p-type doped vertically extending pillar physically contacts the layer.

26. A CMOS inverter comprising:

a p-typed doped single crystal silicon substrate;

a block comprising n-type doped semiconductive material extending into the substrate; at least a portion of the block comprising Si/Ge;

a first transistor device comprising a first gate and a pair of first source/drain regions proximate the first gate; the first gate being over the block; the pair of first source/drain regions extending into the Si/Ge; the first transistor device being a PFET device and the first source/drain regions being p-type doped regions of the Si/Ge of the block;

a layer comprising Si/Ge over the first transistor device; and

a second transistor device supported by the layer comprising Si/Ge, the second transistor device comprising a second gate and a pair of second source/drain regions proximate the second gate, the second transistor device being an NFET device and the second source/drain regions being n-type doped regions of the Si/Ge of the layer.

27. The inverter of claim 26 wherein the Si/Ge of the block is a single crystal.

28. The inverter of claim 26 wherein only a portion of the block comprises Si/Ge; and wherein the block comprises a portion consisting of n-type doped silicon beneath the portion comprising Si/Ge.

29. The inverter of claim 28 the Si/Ge portion of the block is single crystal and wherein the portion consisting of n-type doped silicon is single crystal.

30. The inverter of claim 26 wherein the Si/Ge of the layer is a single crystal.

31. The inverter of claim 26 wherein the layer comprising Si/Ge is a first layer, and wherein the Si/Ge of the first layer is a single crystal having a relaxed crystalline lattice, the inverter further comprising a layer having a strained crystalline lattice between the first layer and the second gate, the layer having the strained crystalline lattice being a second layer.

32. The inverter of claim 31 wherein the second layer consists of silicon or doped silicon.

33. The inverter of claim 31 wherein the second layer consists of Si/Ge or doped Si/Ge.

34. The inverter of claim 26 wherein the Si/Ge of the layer is polycrystalline, wherein the second transistor device comprises an active area extending into the Si/Ge of the layer, the active area including the source/drain regions and a channel region between the source/drain regions; and wherein the portion of the active area within the Si/Ge of the layer is entirely contained within a single crystal of the polycrystalline Si/Ge.

35. A CMOS inverter comprising:

a substrate;

a crystalline layer comprising silicon and germanium supported by the substrate;

a first transistor device supported by the crystalline layer, the first transistor device comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the crystalline layer; an entirety of the first active region within the crystalline layer being within a single crystal of the crystalline layer;

a second transistor device supported by the substrate, the second transistor device comprising a second gate and a second active region proximate the second gate; the second active region including a second channel region and a pair of second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with an input to the inverter; and

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with an output from the inverter.

36. The inverter of claim 35 wherein the crystalline layer is separated from the substrate by an insulative material.

37. The inverter of claim 36 wherein the substrate comprises a semiconductive material.

38. The inverter of claim 36 wherein the substrate comprises glass.

39. The inverter of claim 36 wherein the substrate comprises aluminum oxide.

40. The inverter of claim 36 wherein the substrate comprises silicon dioxide.

41. The inverter of claim 36 wherein the substrate comprises a metal.

42. The inverter of claim 36 wherein the substrate comprises a plastic.

43. The inverter of claim 35 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the crystalline layer and the first transistor device gate.

44. The inverter of claim 43 wherein the strained crystalline lattice layer includes silicon.

45. The inverter of claim 44 wherein the first transistor device is an NFET device.

46. The inverter of claim 44 wherein the first transistor device is a PFET device.

47. The inverter of claim 43 wherein the strained crystalline lattice layer includes silicon and germanium.

48. The inverter of claim 47 wherein the transistor device is a PFET device.

49. The inverter of claim 43 wherein the entirety of the relaxed crystalline lattice is a single crystal.

50. The inverter of claim 43 wherein the relaxed crystalline lattice is polycrystalline.

51. The inverter of claim 43 wherein the relaxed crystalline lattice consists of Si/Ge or doped Si/Ge.

52. The inverter of claim 51 wherein the relaxed crystalline lattice comprises from about 10 to about 60 atomic percent germanium.

53. A CMOS inverter comprising:

a p-type doped semiconductive structure over a substrate;

an NFET device supported by the p-type semiconductive structure, the NFET device comprising an n-type doped source/drain region;

a PFET device supported by the substrate, the PFET device comprising a p-type doped source/drain region;

the p-type doped source/drain region being electrically connected with the n-type doped source/drain region;

the electrical connection from the p-type doped source/drain region to the n-type source/drain region comprising a p-type doped pillar extending from the p-type doped source/drain region to the p-type doped semiconductive structure; the p-type doped pillar comprising at least two portions which are doped to different concentrations relative to one another; one of the portions being nearer the p-type doped source/drain region than the other, and being more heavily doped than said other portion.

54. The inverter of claim 53 wherein the p-type doped semiconductive structure comprises a crystalline layer containing p-type doped Si/Ge over a crystalline layer of p-type doped Si.

55. The inverter of claim 54 wherein the crystalline layer of p-type doped silicon is more heavily doped than said other portion of the p-type doped pillar.

56. The inverter of claim 53 wherein the p-type doped pillar consists of p-type doped silicon.

57. The inverter of claim 53 wherein the semiconductive structure includes Si/Ge.

58. The inverter of claim 57 wherein the Si/Ge comprises from about 10 to about 60 atomic percent germanium.

59. The inverter of claim 53 wherein the substrate comprises n-type doped monocrystalline silicon, and wherein the PFET device comprises a channel region within the n-type doped monocrystalline silicon.

60. The inverter of claim 53 wherein the substrate comprises n-type doped monocrystalline Si/Ge, and wherein the PFET device comprises a channel region within the n-type doped monocrystalline Si/Ge.

61. A CMOS inverter comprising:

a substrate;

a crystalline structure supported by the substrate and comprising a first p-type doped semiconductive material;

an NFET transistor device supported by the crystalline structure, the NFET transistor device comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of n-type doped source/drain regions; at least a portion of the first active region being within the crystalline structure;

a PFET transistor device supported by the substrate, the PFET transistor device comprising a second gate and a second active region proximate the second gate; the second active region including a second channel region and a pair of p-type doped source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with an input to the inverter;

one of the p-type doped source/drain regions being electrically connected with one of the n-type doped source/drain regions and being in electrical connection with an output from the inverter;

the electrical connection from said one of the p-type doped source/drain regions to said one of the n-type source/drain regions comprising a second p-type doped semiconductive material and a third p-type doped semiconductive material; the second p-type doped semiconductive material extending from said one of the p-type doped source/drain regions, and the third p-type doped semiconductive material extending from the second p-type doped semiconductive material to the first p-type doped semiconductive material; the p-

type doped source drain regions being more heavily doped than the second p-type doped semiconductive material, and the second p-type doped semiconductive material being more heavily doped than the third p-type doped semiconductive material.

62. The inverter of claim 61 wherein the first p-type doped semiconductive material is more heavily doped than the third p-type doped semiconductive material.

63. The inverter of claim 61 wherein the crystalline structure includes a first layer comprising conductively-doped silicon; a second layer having a relaxed crystalline lattice, and a third layer having a strained crystalline lattice; the first p-type doped semiconductive material corresponding to any one of the first, second and third layers.

64. The inverter of claim 61 wherein the crystalline structure includes a first layer having a relaxed crystalline lattice, and a second layer having a strained crystalline lattice; the second layer being between the first layer and the first transistor device gate; the p-type doped semiconductive material corresponding to either one of the first and second layers.

65. The inverter of claim 64 wherein the first layer comprises silicon and germanium.

66. The inverter of claim 64 wherein the second layer includes silicon.

67. The inverter of claim 64 wherein the second layer includes silicon and germanium.

68. The inverter of claim 64 wherein the entirety of the first layer is a single crystal.

69. The inverter of claim 64 wherein the first layer is polycrystalline.

70. The inverter of claim 64 wherein the first layer consists of doped Si/Ge.

71. A computer system comprising:

a signal source arranged to provide a data signal; and

an inverter coupled with the signal source, configured to invert the data signal and arranged to output the inverted signal; the inverter including:

a crystalline layer comprising silicon and germanium;

a first transistor device supported by the crystalline layer, the first transistor device comprising a first gate and a first active region proximate the first gate; the first active region including a first channel region and a pair of first source/drain regions; at least a portion of the first active region being within the crystalline layer; an entirety of the first active region within the crystalline layer being within a single crystal of the crystalline layer;

a second transistor device, the second transistor device comprising a second gate and a pair of second source/drain regions;

the first and second gates being electrically connected to one another, and being in electrical connection with the signal source; and

one of the first source/drain regions being electrically connected with one of the second source/drain regions and being in electrical connection with the output.

72. The computer system of claim 71 wherein the crystalline layer has a relaxed crystalline lattice, and further comprising a strained crystalline lattice layer between the crystalline layer and the first transistor device gate.

73. The computer system of claim 72 wherein the strained crystalline lattice layer includes silicon.

74. The computer system of claim 73 wherein the first transistor device is an NFET device.

75. The computer system of claim 73 wherein the first transistor device is a PFET device.

76. The computer system of claim 72 wherein the strained crystalline lattice layer includes silicon and germanium.

77. The computer system of claim 76 wherein the transistor device is a PFET device.

78. The computer system of claim 72 wherein the entirety of the relaxed crystalline lattice is a single crystal.

79. The computer system of claim 72 wherein the relaxed crystalline lattice is polycrystalline.

80. The computer system of claim 72 wherein the relaxed crystalline lattice includes Si/Ge.

81. The computer system of claim 80 wherein the relaxed crystalline lattice comprises from about 10 to about 60 atomic percent germanium.

82. A method of forming a CMOS inverter, comprising:

providing a substrate;

forming a PFET device supported by the substrate, the PFET device comprising a gate and a p-type doped source/drain region proximate the gate;

epitaxially growing a semiconductive material pillar over the p-type source/drain region;

doping the pillar with p-type dopant;

epitaxially growing a silicon-containing seed layer over the pillar;

forming crystalline Si/Ge over the silicon-containing seed layer; and

forming an NFET device supported by the crystalline Si/Ge, the NFET device comprising a gate and an n-type doped source/drain region proximate the gate; and

the pillar being an electrical connection from the p-type doped source/drain region to the n-type source/drain region.

83. The method of claim 82 wherein the doping of the pillar comprises out-diffusion of dopant from the p-type doped source/drain region.

84. The method of claim 82 wherein the forming the crystalline Si/Ge comprises metal-induced lateral recrystallization.

85. The method of claim 82 wherein the crystalline Si/Ge comprises a relaxed crystalline lattice, and further comprising forming a semiconductive material having a strained crystalline lattice over the Si/Ge; the NFET device gate being formed over the material having the strained crystalline lattice and having a channel region extending into the material having the strained crystalline lattice.

86. The method of claim 85 wherein the material having the strained crystalline lattice includes silicon.

87. The method of claim 85 wherein the material having the strained crystalline lattice includes silicon and germanium.

88. The method of claim 85 further comprising doping the epitaxially grown seed layer with p-type dopant.